Integration Manual

HW 86012

DECT
Embedded Radio Module

Version 1.00

DATA UNWIRED

HÖFT & WESSEL

Contents

1. Preface

Dear customer, thank you for choosing the HW 86012 DECT radio module. You have made a good choice, since HW 86012 is a powerful and very versatile product that easily adds DECT communication to your application.

Höft & Wessel aims for best customer satisfaction. In case of any problems with this manual or with our products please do not hesitate to contact us. Your feedback will enable our specialists to solve your problems and continually improve our products and documentation.

1.1 About this document

This manual contains the full technical specification of the HW 86012 as well as all necessary information for a successful hardware integration. It will help you in getting the optimum integration result.

HW 86012 is a future-proof product which offers a number of flexible interfaces and features. It is delivered together with Höft & Wessel DECT firmware. However, not all of the versatile features described in the hardware section are supported by the standard firmware but some will require a customised firmware.

1.2 Related Documents

Refer to HW 86012 Firmware Manual for detailed information on software integration and configuration command reference.

1.3 Contact Höft & Wessel AG

For immediate assistance please address yourself to the Höft & Wessel service line:

Phone: +49-1803-232829
Fax: +49-511-6102-411
Email: info@hoeft-wessel.de

If you have general questions concerning Höft & Wessel Data-Unwired products you may directly contact the Data-Unwired team:

Phone: +49-511-6102-226
Fax: +49-511-6102-437
Email: tol@hoeft-wessel.de

Latest revisions of all publicly available documentation and firmware downloads are available from our web-site www.data-unwired.com. If you are interested in Höft & Wessel Group in general, visit www.hoeft-wessel.com.

Address:

Höft & Wessel AG
Rotenburger Strasse 20
D-30659 Hannover
Germany

2. Important User information

NOTE:

This equipment makes use of radio spectrum and emits radio frequency energy. Care should be taken when the device is integrated in systems. Make sure that all specification within this document are followed, especially concerning operating temperature and supply voltage range.

Refer to national regulations of the region where the HW 86012 module shall be operated and make sure the national requirements are fulfilled.

NOTE:

This equipment is sensitive to electro-static discharge. Use an ESD-safe workstation for handling and use suitable packaging.

3. Introduction

The DECT radio module HW 86012 is a highly versatile and powerful engine for industrial applications. It provides a complete radio according to DECT standard together with a combined DECT baseband and application processor interfacing the host system.

3.1 General description

Built around a 16-bit high-speed low-power RISC microcontroller and a highly integrated state-of-the-art DECT radio the architecture of the HW 86012 features a full set of useful interfaces for support of data and voice services in various environments.

These include RS-232 and SPI for data transmission. Additional general purpose I/Os, I2C plus an accessible bus interface make the HW 86012 ideally suited for industrial automation and control applications with specific I/O requirements. A PCM interface allows for connection to digital voice systems and an analogue front-end supports direct connection of voice equipment such as headsets.

The RF section complies with DECT standard for operation on the European DECT band as well as on most bands used throughout the world. Two antenna ports allow for the use of diversity antennas to improve radio performance in difficult environments.

DECT protocol stack and application software is integrated in the HW 86012 firmware and can be upgraded in the field.

The single-sided ultra-compact and low-power design make the HW 86012 optimally suited for battery powered and handheld devices.

3.2 System diagram

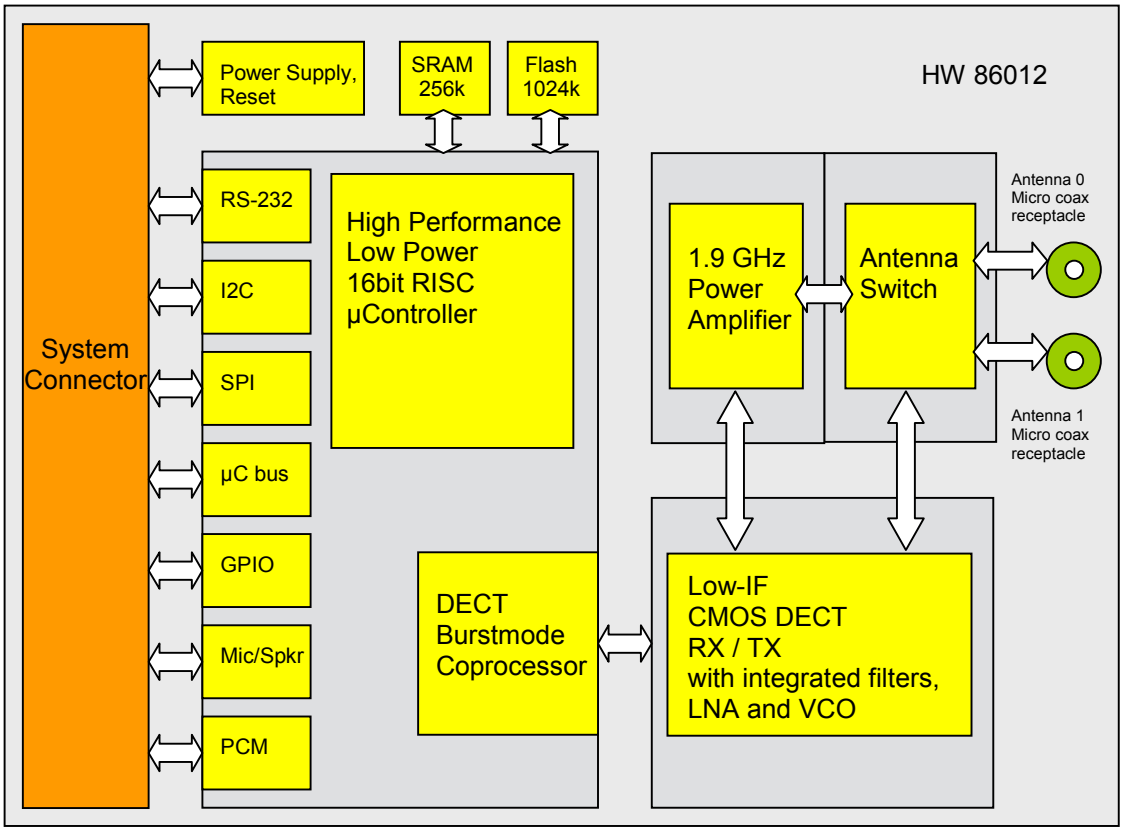


Figure 1: HW86012 System Diagram

3.3 Conformity

The HW 86012 module complies with the essential requirements of §3 and the other relevant provisions of Article 3 of the R&TTE directive when used for its intended purpose and is labelled with the CE conformity mark.

Certification

EN 301406	Digital Enhanced Cordless Telecommunications (DECT); Harmonised EN for Digital Enhanced CordlessTelecommunications (DECT) covering essential requirements under article 3.2 of the R&TTE Directive; Generic radio
EN 301489-1	Electromagnetic compatibility and Radio spectrum Matters (ERM); ElectroMagnetic Compatibility (EMC) standard for radio equipment and services; Part 1: Common technical requirements
EN 301489-6	Electromagnetic compatibility and Radio spectrum Matters (ERM); ElectroMagnetic Compatibility (EMC) standard for radio equipment and services; Part 6: Specific conditions for Digital Enhanced Cordless Telecommunications (DECT) equipment
EN 61000-4-3	Electromagnetic compatibility (EMC) - Part 4-3: Testing and measurement techniques - Radiated, radio-frequency, electromagnetic field immunity test
EN 60950-1	Safety of information technology equipment

Standards

ETSI EN 301175	Digital Enhanced Cordless Telecommunications (DECT); Common Interface (CI);

HÖFT & WESSEL

CE

EU – Konformitätserklärung
EC - Declaration of Conformity

gemäß dem Gesetz über Funkanlagen und Telekommunikationsendeinrichtungen (FTEG) und der Richtlinie 1999/5/EG (R&TTE)
in accordance with the Radio and Telecommunications Terminal Equipment Act (FTEG) and Directive 1999/5/EC (R&TTE Directive)

Hersteller / Manufacturer:	Höft & Wessel AG
Anschrift / Address:	Rotenburger Straße 20, D-30659 Hannover, Germany
Produkt / Product:	Embedded DECT-Modul
Typ / Type:	**HW 86012**

☐ Telekommunikations-Endeinrichtung
Telecommunications terminal equipment

☒ Funkeinrichtung
Radio equipment

Geräteklasse:
Equipment class

Höft & Wessel AG erklärt, dass das bezeichnete Produkt bei bestimmungsgemäßer Verwendung den grundlegenden Anforderungen des § 3 und den übrigen einschlägigen Bestimmungen des FTEG (Artikel 3 der R&TTE-Richtlinie) entspricht.
Höft & Wessel AG declares that the product complies with the essential requirements of §3 and the other relevant provisions of the FTEG (Article 3 of the R&TTE Directive) when used for its intended purpose

Angewendete harmonisierte Normen / Harmonised standards applied:

Luftschnittstelle bei Funkanlagen gemäß § 3 (2) ((Artikel 3 (2))
Air interface of the radio systems pursuant to article 3 (2)

EN 301406 V 1.5.1 (2003)

Schutzanforderungen in Bezug auf die elektromagnetische Verträglichkeit § 3 (1) 2 (Artikel 3 (1) b))
Protection requirements concerning electromagnetic compatibility according to article 3 (1) b

EN 301489-1 : V1.6.1 (2005), EN 301489-6 : V1.2.1 (2002), EN 61000-4-3 : 2002+A1:2002

Gesundheit und Sicherheit gemäß § 3 (1) 1 (Artikel 3 (1) a))
Health and safety requirements pursuant to article 3 (1) a

EN 60950-1 2001

Hannover, den 23.03.06
Place and date

Rechtsverbindliche Unterschrift
Name and signature

.....

Peter Claussen
Höft & Wessel AG

4. Hardware Description

4.1 Mechanical Characteristics

4.1.1 Dimensions

Parameter	Typ.	unit
Length	52.0	mm
Width	37.0	mm
Height	3.2	mm

4.1.2 Weight

Parameter	Typ.	unit
Weight	8.3	g

4.1.3 Image

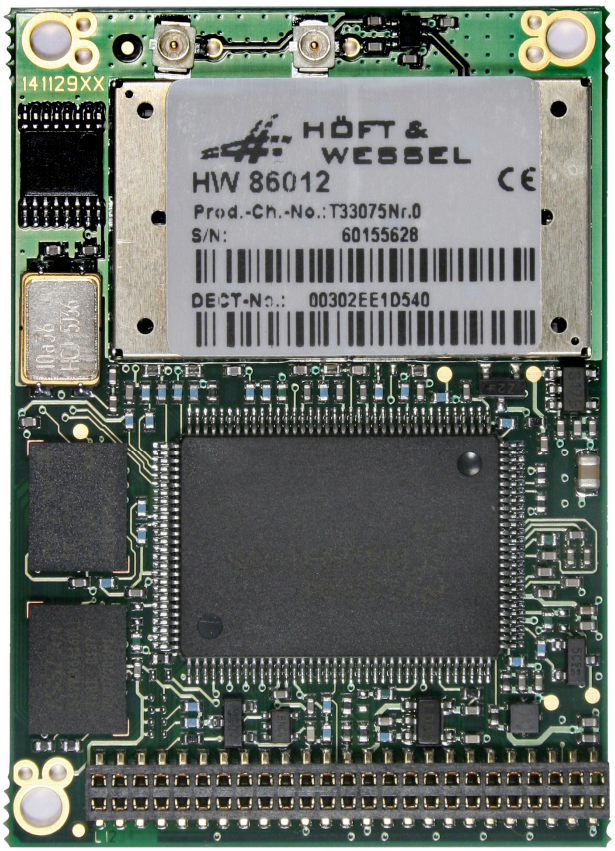
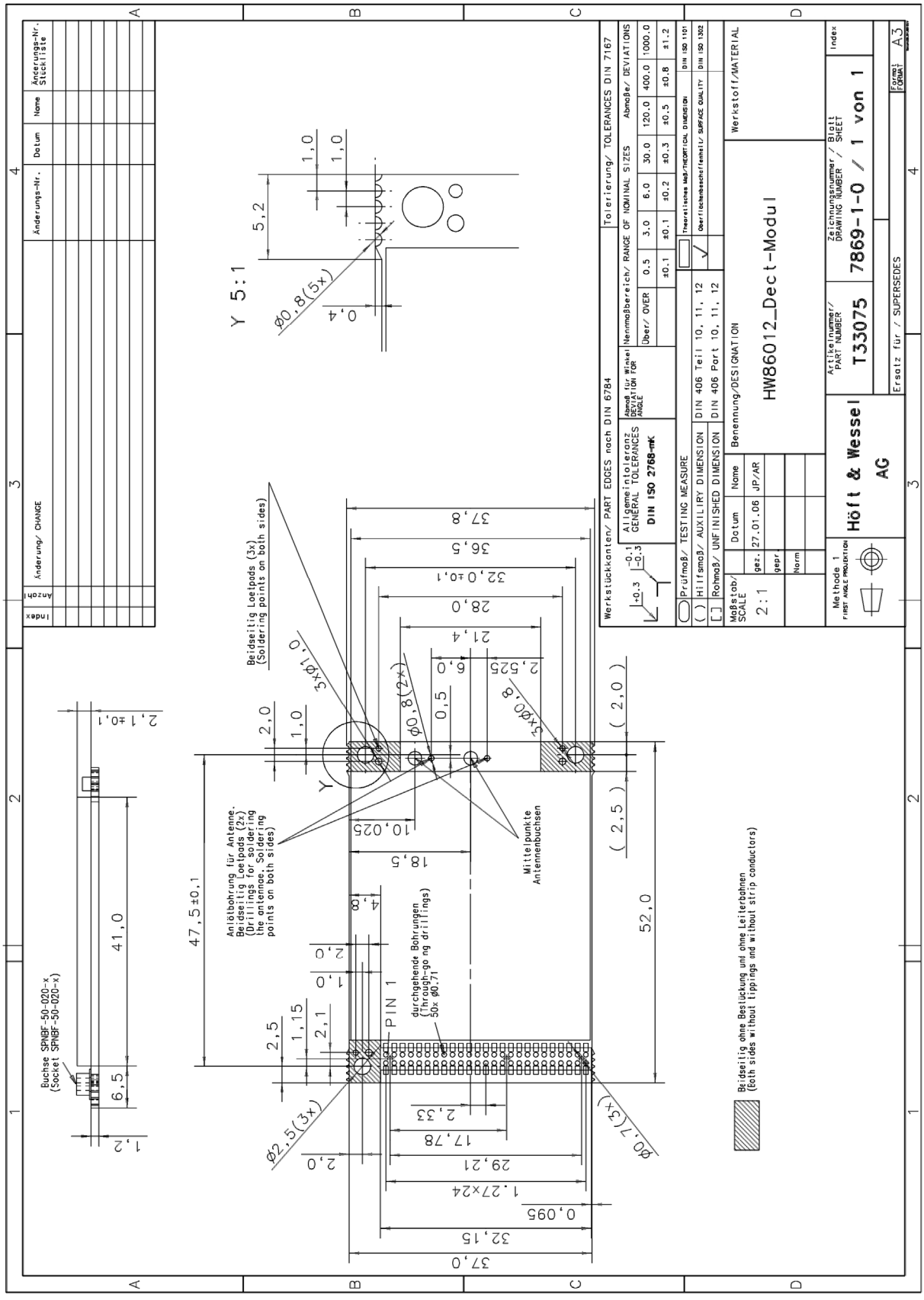


Figure 2: Image

4.1.4 Mechanical Drawing



4.2 Electrical Characteristics

4.2.1 Pinout

Pin	Name	Description	Pintype	reset state
1	VXN	Speaker out negative	Analogue	Oa
2	VXP	Speaker out positive	Analogue	Oa
3	VXIN	Microphone in negative	Analogue	Ia
4	VXIP	Microphone in positive	Analogue	Ia
5	MICN	Microphone bias out reference	Analogue	Oa
6	MICP	Microphone bias out positive	Analogue	Oa
7	RSTNO	Reset out	Digital	Ipu80k
8	RINGP/SPIDI	Ring out, SPI data in	Digital	I
9	ADC/GPIO12	Analogue digital converter in, General purpose I/O	Dig/Analogue	I
10	PWM/SPICLK	PWM out, SPI clock in/out, General purpose I/O	Digital	I
11	SDA/PCMFSC1/GPIO11	I2C Data, PCM frame sync 1, General purpose I/O	Digital	Ipu
12	SCL/GPIO10	I2C Clock, General purpose I/O	Digital	O1
13	GPIO1/LED0	General purpose I/O, LED0 control	Digital	O1
14	GPIO2/SPIDO/LED1	General purpose O, SPI data out, LED1 control	Digital	O0
15	GPIO3/PCMFSC0	General purpose I/O, PCM frame sync 0	Digital	Ipu
16	GPIO4/PCMCLK	General purpose I/O, PCM clock in/out	Digital	Ipu
17	GPIO5/PCMDIN	General purpose I/O, PCM data in	Digital	Ipu
18	GPIO6/PCMDOUT	General purpose I/O, PCM data out	Digital	Ipu
19	GPIO7/EXTINT/PIWRDY	General purpose I/O, external interrupt request in, parallel interface write ready	Digital	Ipu
20	GPIO8/EXTCS/PICS	General purpose I/O, external chip select out, parallel interface select	Digital	Ipu
21	RSTBI	Reset in	Digital	Ipu
22	GND	Ground	Ground	
23	RTSI/PIRDREQ/BOOT2	RS232 RST in, parallel interface read request, mode select in	Digital	Ipu
24	DTRI/BOOT3	RS232 DTR in, mode select in	Digital	Ipu
25	RXDO	RS232 RXD out	Digital	Ipu
26	TXDI	RS232 TXD in	Digital	I
27	V3P3	Digital section power supply	Supply	
28	VBATP	RF section power supply	Supply	
29	CTSO/BOOT0	RS232 CTS out, mode select in	Digital	Ipu
30	DSRO/BOOT1	RS232 DSR out, mode select in	Digital	Ipu
31	DCDIO	RS232 DCD in/out, General purpose I/O	Digital	Ohzpu
32	RIIO	RS232 RI in/out, General purpose I/O	Digital	Ohzpu
33	RDn	µC bus read	Digital	O1
34	WRn	µC bus write	Digital	O1
35	D0	µC bus data	Digital	O1
36	D1	µC bus data	Digital	O1
37	D2	µC bus data	Digital	O1
38	D3	µC bus data	Digital	O1
39	D4	µC bus data	Digital	O1
40	D5	µC bus data	Digital	O1
41	D6	µC bus data	Digital	O1
42	D7	µC bus data	Digital	O1
43	A0	µC bus address	Digital	O1
44	A1	µC bus address	Digital	O1
45	A2	µC bus address	Digital	O1
46	A3	µC bus address	Digital	O1
47	A4	µC bus address	Digital	O1
48	A5	µC bus address	Digital	O1
49	GPIO9	General purpose I/O	Digital	Ohz
50	GND	Ground	Ground	

Legend: Oa - analogue output, Ia - analogue input, Ipu - digital input with internal pull-up, Ipu80k - digital input with 80kOhm pull-up - digital input w/o pull-up, O1 - digital ouput high state, O0 - digital output low state, Ohz - digital ouput high impedance state, Ohzpu - digital output high impedance state with pullup.

4.2.2 Absolute Maximum Ratings

Parameter	Remarks	Conditions	Min	Max	unit
V3P3	Digital supply voltage		-0.3	4.0	V
VBATP	RF supply voltage		-0.3	4.6	V
Iiosum	Current through all IO pins			90	mA
Iio	Current through IO pin			20	mA
Vdigin	Max Voltage on any digital inputs	V3P3>=3.3V V3P3<3,3V	-0.3 -0.3	3.6 V3P3+0.3	V
Vanain	Max voltage on any analogue inputs		-0.3	2.0	V
Iioprot	Max current through any pin's protection diodes to V3P3			100	µA
Imicprot	Max current through MIC input pin's protection diodes			2.4	mA

NOTE: Absolute maximum ratings may be applied to the module for a short period of time. Applying values greater than those mentioned will damage the module.

4.2.3 Electrical Specifications

4.2.3.1 Power Supply

Parameter	Remarks	Conditions	Min	Typ.	Max	unit
V3P3	Digital supply voltage		3.1	3.3	3.5	V
VBATP	RF supply voltage		3.0		4.6	V
VBATP_ripple	Ripple on VBATP				100	mV
I3P3	Digital supply current	CO Idle 1-bearer CLDPS Idle 115kbps		 15..20 21..23 15..23 30..37	 75	mA
IBATP	RF supply current	CO PT Scan PT Sync'ed PT 1-bearer FT Idle FT 1-bearer CLDPS PT Scan PT Sync'ed 0kbps PT RX 115kbps PT TX 115kbps FT Idle 0kbps FT RX 115kbps FT TX 115kbps Continuous Receive Continuous Transmit		 99 8 14 33 40 99 15 50 67 26..65 69 96 99 230	 400	mA

NOTE: Maximum IBATP current during transmission may increase in case of antenna impedance mismatch. CO and CLDPS measurements with P32 slot format operation.

4.2.3.2 Digital I/O

Parameter	Remarks	Conditions	Min	Typ.	Max	unit
Vin_dig_high	Digital in high level		2.0			V
Vin_dig_low	Digital in low level				1.0 (GPIO9:0.6)	V
Vout_dig_low_100µ	Digital out low level	100µA			0.1	V
Vout_dig_low_8m	Digital out low level	8mA			0.6	V
Vout_dig_high_100µ	Digital out high level	100µA	3.0			V
Vout_dig_high_8m	Digital out high level	8mA	2.4			V

4.2.3.3 UART interface

Parameter	Remarks	Conditions	Min	Typ.	Max	unit
UART data rates	Default: 115.2 kbps in data mode, 9.6 kbps in hardware configuration mode			230.4 115.2 57.6 38.4 19.2 9.6		kBd
UART framing				8N1		
UART buffer				DMA, software controlled		

4.2.3.4 SPI interface

SPI interface will be operated in Master mode.

Parameter	Remarks	Conditions	Min	Typ.	Max	unit
SPI Clock Master				1.296 2.592 5.184		MHz
SPI Clock Slave					5.184	MHz
SPI Mode				0, 1, 2, 3		

4.2.3.5 Radio Frequency Interface

Parameter	Remarks	Conditions	Min	Typ.	Max	unit
Frequency range	Software controlled	ETSI	1870 1880		1930 1900	MHz
Channel spacing				1.728		MHz
Frequency offset			-50	0	+50	kHz
Frequency drift			-16	-30	-41	kHz/ms
Transmitter output power	Software controlled	ETSI FCC	20.0 17.0	23.0 20.0	24.0 21.0	dBm
Receiver sensitivity	BER < 10e-3		-96	-93	-90	dBm
Antenna ports impedance				50		Ohm
Isolation between antenna ports			10	25		dB
Modulation			Gaussian Frequency Shift Keying (GFSK: BxT=0.5 ; m= 288kHz)			
Deviation			280		400	kHz
Multiplexing			Time Division Multiple Access (TDMA)			
Bearers	blind slot radio	connection oriented	6 full-slot duplex bearers			
Air data rate			1.152			Mbps
User data rate	per radio cell	CLDPS	up to 500			kbps
	per bearer	connection oriented	26			kbps

4.2.3.6 Voice interface

4.2.3.6.1 Microphone bias

Parameter	Remarks	Conditions	Min	Typ.	Max	unit
Vref	Differential voltage between MICP and MICN pins			1.5		V
Vrefp_acc	Accuracy of MICP voltage	Trimmed	-1		+1	%
Vrefn_m	Voltage from MICN to GND			0		V
Vrefp_load c	MICP load capacitance				20	pF
Rvrefp	MICP output resistance			10	15	Ohm
Nrefp	MICP peak noise	CCITT weighted		-100	-80	dBV
Srefp	MICP power supply rejection ratio		40			dB
Ivrefp	MICP output current	Minimal load must be applied	100		600	µA

4.2.3.6.2 Microphone input

Parameter	Remarks	Conditions	Min	Typ.	Max	unit
Vmic_0dB	Differential RMS input voltage between VXIP and VXIN for 0dBm0	0dBm0 at codec output = -3.14dB of max PCM value, microphone gain at minimum, @1020Hz		130		mV
Vmic_0dB_acc	Accuracy	Trimmed	-0.5		+0.5	dB
Vmic_cm	VXIP/VXIN common mode voltage			0.9		V
Vmic_gain	Microphone gain	Software controlled, 16 steps	0		30.1	dB
Vmic_gain_acc	Microphone gain accuracy		-0.75		+0.75	dB
Rmic_diff	Differential input impedance between VXIN and VXIP		150			kOhm
Vmic_offset	Input referred DC-offset	Microphone gain at maximum	-2.6		+2.6	mV

4.2.3.6.3 Speaker output

Parameter	Remarks	Conditions	Min	Typ.	Max	unit
Differential RMS output voltage between VXP and VXN		0dBm0 at codec input = -3.14dB from max PCM value, speaker gain = 0.0dB, load circuit acc. to section 0, @1020Hz		0.69		V
Differential Output Impedance between VXP and VXN				2	5	Ohm
Load resistance			30			Ohm
Load capacitance		RL = 00 Rl < 1kohm			100 30	pF
Speaker gain		Software controlled	-12		2.2	dB
Absolute speaker gain accuracy			-0.75		+0.75	dB

4.3 Environmental Conditions

Parameter	Remarks	Conditions	Min	Typ.	Max	unit
Ta_op	Operational temperature		-20	+25	+60	°C
Ta_st	Storage temperature		-40		+80	°C
H	Humidity	Non condensing	0		95	%

4.4 Interface Description

4.4.1 System connector

The interface to the host system is implemented as a 50 pin 1.27mm grid female connector. The part used on the HW 86012 module is a Plastron SPNBF-50-B-0, which is compatible to Samtec CLP-125-02-G-D-BE.

It is recommended to connect the module with a pin header by bottom entry method, i.e. through the printed board. This allows for best space saving and the RF connectors are accessible in mounted position.

Suitable pin header connectors are available from different manufacturers, such as Plastron, Samtec or others. The pin length determines the module's height above the host circuit board, depending whether components shall be fitted underneath the module.

Find a list of parts below as a suggestion. See section 6 of this document for accessories.

Manufacturer	Part No.
Plastron	SPNZ-50...
	SPNB2-50...
Samtech	FTSH125-01...

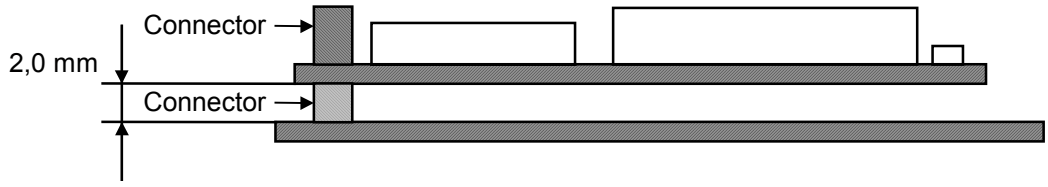


Figure 3: No components fitted on target PCB below HW 86012. Minimum distance between PCBs 2,0 mm

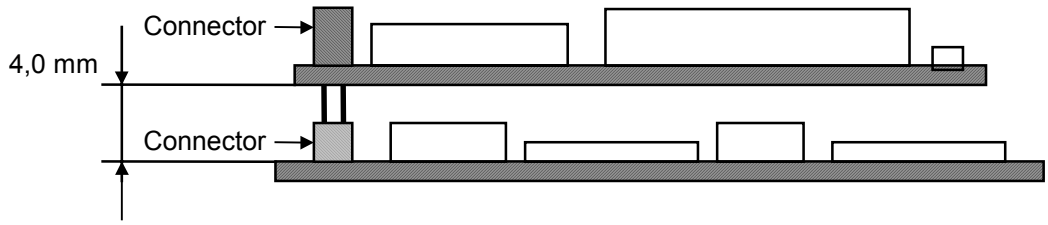


Figure 4: Components fitted on target PCB below HW 86012. Distance between PCBs depend on component heights (here: 4,0 mm)

4.4.2 UART Interface

The HW 86012 module provides a fully featured RS-232 serial interface. All interface signals are 3.3V CMOS level and are active at low state. A V.24 line driver must be provided in order to connect to a standard V.24 device, e.g. a PC.

NOTE!

Connecting the module to a V.24 line without external line drivers may damage the module.

Signal	I/O	Description
TXDI	I	serial data from host to HW 86012
RXDO	O	serial data from HW 86012 to host
RTSI	I	hardware handshake from host to HW 86012
CTSO	O	hardware handshake from HW 86012 to host
DTRI	I	ready signal from host to HW 86012
DSRO	O	ready signal from HW 86012 to host
DCDIO	I/O	carrier detect modem lead signal
RIIO	I/O	ring indicator modem lead signal

Some of the RS-232 signals are used to control mode selection during hardware reset. Refer to section 4.4.6 for details. Most lead signals have enhanced functionality depending on software configuration. Refer to HW 86012 Firmware Manual for a detailed description.

NOTE!

The UART interface does not support the transmission of break signals as these have a special purpose function in Höft & Wessel devices. Do not apply break conditions unless specified by Höft & Wessel. Make sure that a break condition is not applied during power-up transient conditions.

4.4.2.1 Minimum RS-232 configuration

The RS-232 interface may also be used in reduced configurations.

3-wire (RXDO,TXDI,GND) interface

- no hardware handshake, no call control
- requires to disable hardware handshake (see command „SPCOM“ in HW 86012 Firmware Manual for details) and call control (command „SPCC“).

5-wire interface (RXDO,TXDI,RTSI,CTSO,GND)

- hardware handshake, no call control
- requires to disable call control (see command „SPCC“ in HW 86012 Firmware Manual for details)

4.4.3 SPI Interface

The Serial Programming Interface provides a performant serial interface to control the module and for user data transfer. The module will act as SPI master device and therefore control SPI clock.

Signal	I/O	Description
SPIDO	O	SPI data out
SPIDI	I	SPI data in
SPICLK	I/O	SPI clock

This feature is not supported in standard firmware release.

4.4.4 Voice Interface

Analogue voice interface is provided by hardware. The interface provides differential input and output as well as microphone bias generation and is suitable for connecting differential mode handsets or headsets.

Signal	I/O	Description
VXOP	O	analogue speaker output positive
VXON	O	analogue speaker output negative
VXIP	I	analogue microphone input positive
VXIN	I	analogue microphone input negative
MICBP	O	microphone bias voltage positive
MICBN	O	microphone bias voltage negative

4.4.4.1 Connection of microphone and speaker

Figure 3 shows a typical circuit to connect speaker and electret microphone.

The values of the components must be chosen such that

- Together with the input impedance of the pre-amplifier the AC coupling capacitors C1 and C2 form a transfer function with a zero at a frequency low enough to avoid unacceptable ripples in the considered signal bandwidth.
- A very low frequency pole (below 50 Hz) is formed by the capacitor C4 and the series resistors R1 and R2.
- The microphone biasing current is set such that the required sensitivity target is met. This depends on the microphone characteristics.
- System performance may be further enhanced by an additional capacitor C3 that filters out the peak of the cavity resonance. The value depends on the physical characteristics of the microphone housing.

Component values in Figure 1 are typical for a low impedance microphone (less than 3 kΩ).

Note that all signals are dc-coupled to the microcontroller.

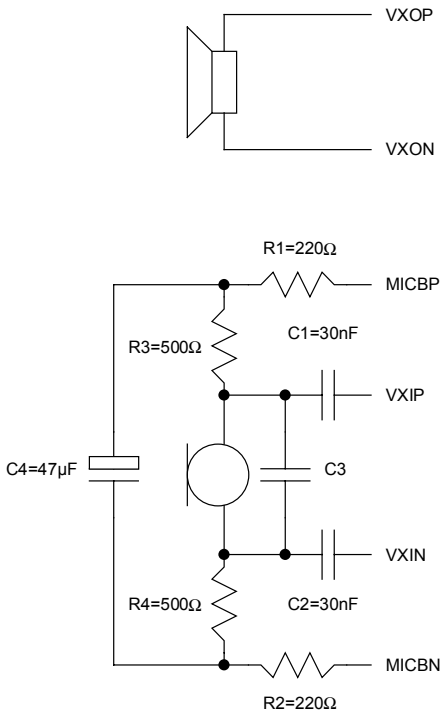


Figure 5: Electrical connection of microphone and speaker

4.4.5 ADC/PWM Interface

This interface is used to capture and reproduce analogue signals with low bandwidth.

Signal	I/O	Description
ADC	I	analogue / digital converter in
PWM	O	pulse width modulated output

This feature is not supported in standard firmware releases.

4.4.6 Reset Interface

The reset interface is used to reset the HW 86012 module and its external peripherals.

Signal	I/O	Description
RSTBI	I	Reset input, ac-coupled, triggers on falling edge
RSTNO	I/O	Reset output, active low, Z=3.3kOhm[1]
BOOT0	I	download mode selection
BOOT1	I	download mode selection
BOOT2	I	data / configuration mode selection
BOOT3	I	data / configuration mode selection

A reset at the HW 86012 module occurs in the following situations:
- Power on reset
- low voltage detected from internal supervisory circuit
- software reset
- external reset through RSTBI signal
- external reset through RSTNO signal (not recommended)

The HW 86012 module may simply be reset through the reset interface, but additionally certain reset sequences are used to change the module's operational modes:

- Data mode – normal operation with user data transfer
- Configuration mode – allows for configuration commands to be entered in order to change the software settings
- Download mode – a new firmware binary may be downloaded to the module's flash memory.

To support theses modes the module must reliably distinguish an external reset from any other reset (collectively referred to as internal resets). This is achieved through appropriate reset timing. The host, which initiates the external reset must pull the RSTBI signal down. This will physically reset the HW 86012 module as can be observed on the RSTNO output.

After termination of its internal reset cycle, the HW 86012 will raise the RSTNO signal and firmware starts execution. In an early stage of program execution the firmware will test the value of the RSTBI signal. An external reset is indicated by a logical low.

At power-up the HW 86012 is automatically reset by the internal supervisory circuit.

A reset by the host processor (using the RSTBI signal) is needed in order to:
- start **configuration mode** (however, a software configuration mode may be entered by applying an escape sequence, see HW 86012 Firmware Manual).
- start **download mode** (however, the download procedure may also be invoked with a special command in configuration mode, see HW 86012 Firmware Manual).
- change from one of the above modes to **data mode** (normal operation), except if the software configuration mode entered by an escape sequence the data mode can be entered with an exit command.

If none of these hardware functions are required by the application, the RSTBI pin may be left open. In any case, taking provisions for potential firmware downloads is a substantial advantage for the future-proofness of your product. Use the configuration mode reset in your application e.g. if you cannot operate at the initial serial speed or want to avoid the escape sequence to be transferred through the data channel. Also, a few commands may not be available during software configuration mode (using the escape sequence).

[1] RSTNO pin is driven by a push-pull output trough a series resitor of 3.3kOhm. Care must be taken when this pin shall be used to control external circuitry as only high impedance inputs shall be connected to ensure proper operation.

4.4.6.1 Reset timing (external reset)

In order to make sure that an external reset is detected correctly by the firmware, the host must pull RSTBI down sufficiently long time. The exact timing requirements are indicated in Figure 6.

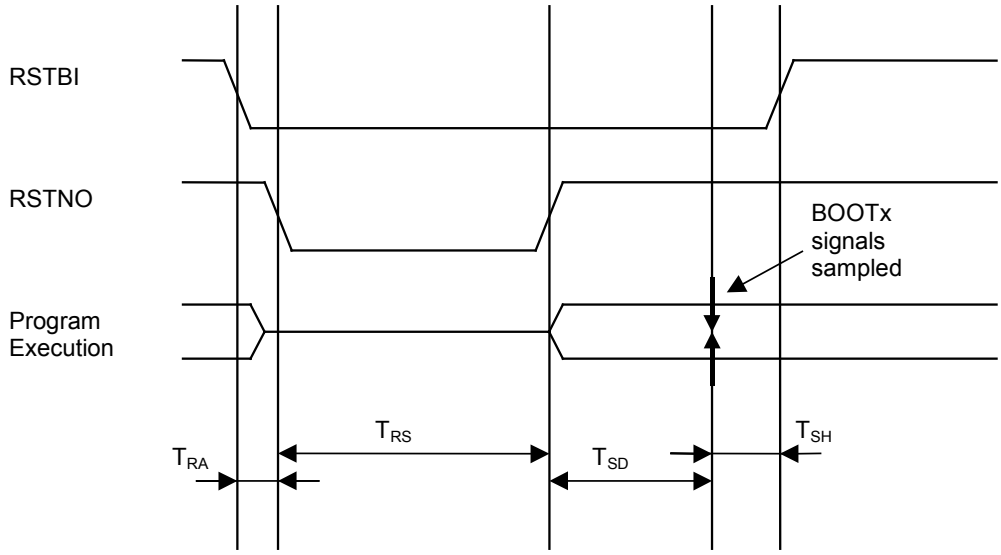


Figure 6: Reset Timing

Parameter	min.	max.
T_{RA}		11 µs
T_{RS}	100 ms	860 ms
T_{SD}	18 µs	100 ms
T_{SH}	100 µs	

The host hardware can be sure to generate external reset pulses of sufficient length, if

- either it observes the RSTNO signal and keeps the RSTBI signal LOW at least 100ms after the rising edge of RSTNO, or
- it applies a RSTBI pulse of at least 960ms.

The latter method is simpler but also slower.

T_{RS} specifies the duration of the reset pulse. It depends on component tolerances, temperature and operating voltage and therefore may be variable.

T_{SD} specifies the time where the status of BOOTx lines is latched. It depends on the firmware implementation and may vary between different firmware versions.

4.4.6.2 Short Reset

A short reset is a low-active RSTBI pulse that is shorter than the RSTNO pulse.

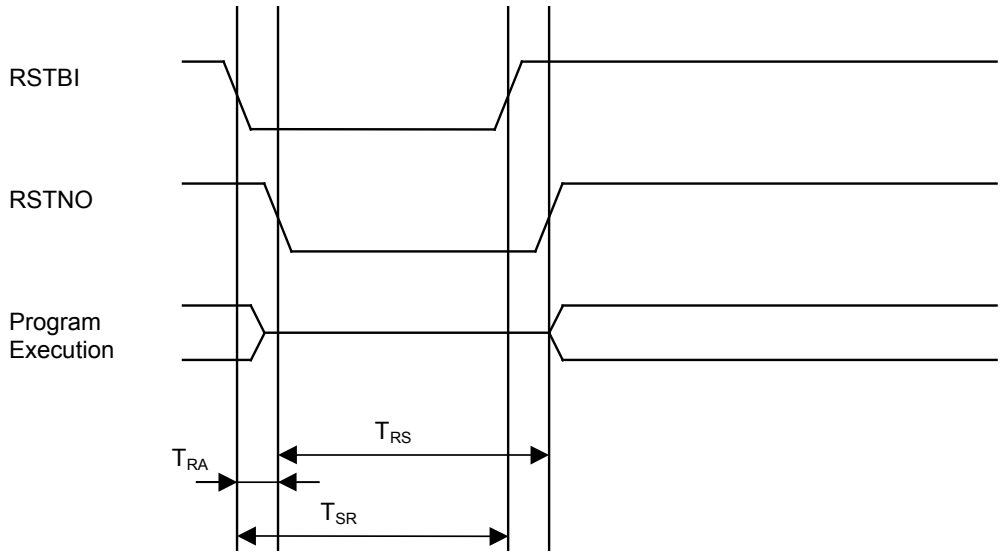


Figure 7: Short Reset

Parameter	min.	max.
T_{SR}	5ms	50ms

Although it is triggered by the RSTBI signal the firmware of the HW 86012 treats a short reset as an internal reset. The host hardware may use this feature to emulate a power-up reset to the HW 86012. A short reset will lead to normal start of firmware unless BOOT0 and BOOT1 pins are pulled low from external circuitry. In this case the download mode is entered.

4.4.6.3 Activation of Download and Configuration Mode

During any reset (internal or external) interface signals BOOT0, BOOT1 overload the normal function of these signals (CTSO, DSRO). They are used to activate download mode if pulled low from external circuitry.

If case of an external reset (RSTBI held low after rising edge of RSTNO) the BOOT2 and BOOT3 signals are evaluated in order to activate configuration mode or normal start of firmware (data mode).

The following table gives an overview on how the modes are selected. Combinations other than specified must not be applied.

RSTBI	BOOT0 (CTSO)	BOOT1 (DSRO)	BOOT2 (RTSI)	BOOT3 (DTRI)	Function
X	LOW	LOW	X	X	Enable firmware **download mode**
LOW	HIGH	HIGH	HIGH	HIGH	Enable firmware **configuration mode**
LOW	HIGH	HIGH	LOW	HIGH	Enable firmware **data mode** (normal operation)
HIGH	HIGH	HIGH	X	X	

X: don't care

RSTBI, BOOT0, BOOT1, BOOT2 and BOOT3 are latched at the rising edge of RSTNO + T_{SD}. All signals have internal pull-ups and may be left unconnected if not used. In order to avoid unwanted switches to firmware download mode, the host device shall take care that BOOT0 and BOOT1 are driven low only together with RSTBI driven low. For normal firmware start RSTBI shall not be held low. In case of external reset BOOT2 and BOOT3 shall be used as normal RS 232 signals after RSTBI is released.

The evaluation kit HW 86916 includes adapter boards that support firmware download and configuration mode reset from a standard PC COM port as well as the required software tools.

4.4.6.4 Precautions to avoid Reset Problems

The host hardware must assure an appropriate environment that avoids unwanted resets. The reset behaviour is a main source of integration problems and requires specific attention.

Please make sure that the following conditions are fulfilled during operation:

- V3P3 must not drop below 2.63 V. This will trigger a low voltage reset.
- At power-up the RSTBI signal should be either high impedance (not connected) or logic HIGH if data mode is required. A logic LOW during power-up may be interpreted as external reset and may result in unwanted mode selection.
- If the host hardware is not able to assure the appropriate RSTBI level during power-up, it may use a short reset afterwards to emulate a power-up reset.
- DSRO and CTSO are outputs of the HW 86012. The host hardware must never actively drive these signals for any other purpose than entering the download mode. They shall only be driven from the host during RSTBI = low.
- The external reset is triggered by the falling edge of the RSTBI signal. Make sure that the fall time (90% down to 10% of V3P3) is less than 50ns.

4.4.7 I2C Interface

I2C Interface is provided by the hardware. This feature is not supported in standard firmware releases.

4.4.8 PCM Interface

PCM Interface is provided by the hardware.

Signal	I/O	Description
PCMCLK	I/O	PCM clock signal in/out
PCMFSC0	I/O	PCM frame sync 0 in/out
PCMFSC1	I/O	PCM frame sync 1 strobe in/out
PCMDIN	I/O	PCM data in/out
PCMDOUT	I/O	PCM data out/out

PCMDIN and PCMDOUT are open drain outputs or inputs without internal pull-ups. External pull-up resistors are required for operation.

This feature is not supported in standard firmware release.

4.4.9 General Purpose I/O

HW 86012 provides 12 general purpose I/O pins GPIO1 to GPIO12. They are enabled by firmware. Since most signals are multiplexed with other interface signals, certain restrictions to the usage of GPIO signals apply.

This feature is not supported in standard firmware release.

4.4.10 LED interface

LED0 and LED1 outputs are provided. They may be used to control two LEDs to display connection and configuration mode and data activity.

Signal	State	Description
LED0	LOW	LED0 off
	HIGH	LED0 on
LED1	LOW	LED1 off
	HIGH	LED1 on

LED0	LED1	Meaning
•	•	Power off condition or firmware download
☼☼••	•	Power on, not connected state related to higher protocol level (slow blink)
☼	•	Connection to base station established, flickers while data is transmitted.
•	☼	Device has entered configuration mode.

Note that current capability is limited so that an external LED driver may be required.

This functionality is deactivated by default and must be activated by software (for details see command „SPUI" in HW 86012 Firmware Manual).

4.4.11 Bus Interface

The bus interface allows for external peripherals to be accessed by the module. The 8-bit data bus and 5-bit address bus, together with control signals, including chip select, DMA and interrupt signals allows for a variety of external peripherals to be accessed by the module.

Signal	I/O	Description
A0 .. A5	O	Address bus
D0 .. D7	I/O	Data bus
RDN	O	Read signal, active low
WRN	O	Read signal, active low
EXTCS	O	Chip select signal, active low
EXTINT	I	Interrupt request signal, active low
PIWRDY	I	Parallel Interface Write Ready
PIRDREQ	O	Parallel Interface Read Request

This feature is not supported in standard firmware release.

4.4.12 RF Interface

RF Interface provides two antenna connections.

The used antenna ports 0 or 1 can be configured by software. In addition the module supports antenna diversity. During reception of data, the module measures the signal strength on both antennas and activates the antenna with highest level for reception of a data packet. This will significantly improve operation for example in multipath environments, utilising the effect that fading is space dependant and one of the two antennas will most probably experience less fading than the other. See HW 86012 Firmware Manual for details on configuration.

The coaxial connector used on the module is a Hirose U.FL series connector, type U.FL-R-SMT, reference no. CL331-0471-0. Refer to www.hirose.com for details.

Adequate cable sets are available with the Hirose connectors already mounted. Contact Höft & Wessel AG for accessories.

On the antenna 0 and 1 solder through holes, a wire antenna may be attached if no external antenna shall be used. The attached antenna can be a quarter wavelength monopole with a length of approx. 38 mm.

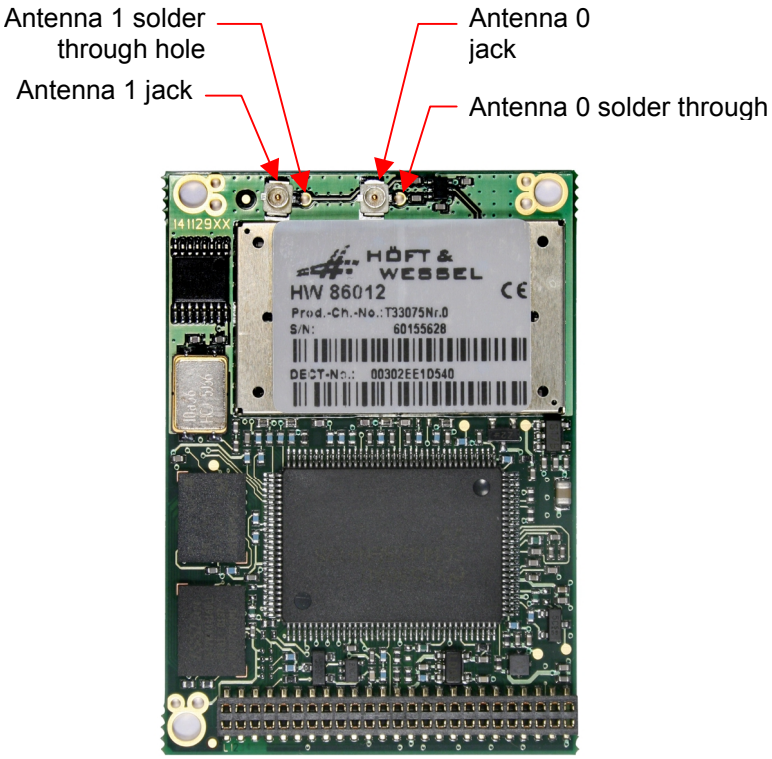


Figure 8: Antenna Ports

NOTE:

Do not use the through hole connection and the coaxial connector of one antenna port at the same time.

NOTE:

Use ESD safe environments for soldering on antenna ports.

Antenna design is the most crucial topic during integration of radio systems. The antenna shall provide good omnidirectional characteristics or a certain directional pattern, depending on the application. Using poor antennas may lead to significant degradation of system performance or influence the reliability. See section 5.3 for recommendations.

In the standard version the HW 86012 module comes with one wire antenna mounted on Antenna 1 solder through hole. This antenna is active in the default configuration.

Figure 9: HW 86012 standard version with wire antenna mounted on ANT1 port.

Wire antenna specification:

Length:	40 mm max.
Diameter:	1.2 mm typ.
Projection top:	3.0 mm max.
Projection bottom:	2.0 mm max.

5. Specific Integration Topics

5.1 Type Approval

A product that uses HW 86012 and is destined for countries of the European Union requires a manufacturer declaration according to the R&TTE directive.

HW 86012 has a type approval according the ETSI EN 301406 standard. This is a mandatory requirement for DECT equipment.

When you integrate HW 86012 in your product, it is not required to perform a complete radio test again. Although it is not mandatory, Höft & Wessel recommends that you have your product checked in a shortened radio spot check with a subset of ETSI EN 301406.

Your product will have to be tested according to EN 301489-1/-6 (EMC for DECT equipment) and LVD.

If you intend to market your product outside the European Union, please check that the respective countries accept the DECT standard and which frequency band applies. Usually a type approval must be performed according to national regulations.

If you require support for the certification process, please address yourself to Höft & Wessel.

5.2 Power Supply

There a two power supply rails. V3P3 supplies digital section including processor, memories and DECT baseband with a medium current draw, while VBATP supplies the RF transceiver and power amplifier with a high peak pulsed current draw.

Especially the VBATP power supply must be chosen so that the maximum current during transmit pulses can be delivered. Keep in mind that an antenna which is not sufficiently matched to the transmitter impedance may significantly increase the transmitter current draw.

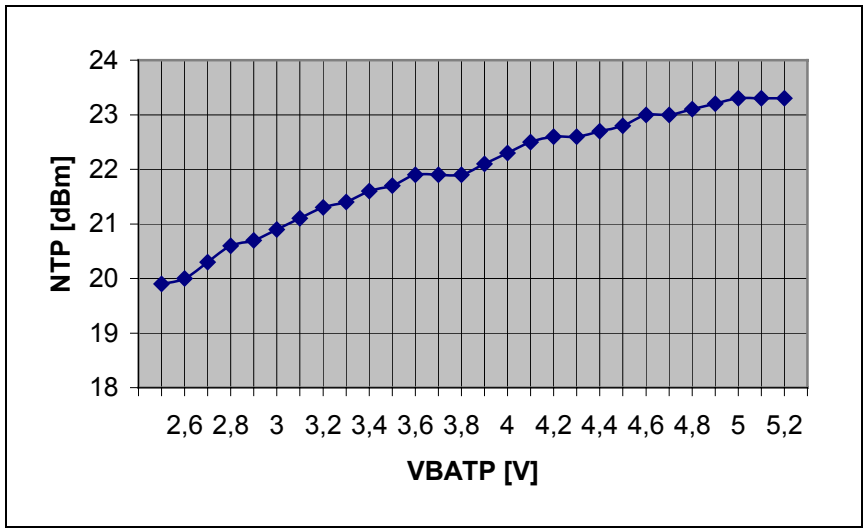


Figure 10: Nominal Transmit Power (NTP) vs VBATP supply voltage

Both power supply rails are designed to work at 3.3 V nominal and may therefore be supplied by the same current source. The higher voltages specified for VBATP will enable compatibility to HW 86010 and HW 86020 modules. However, the RF power output is a function of VBATP as shown in Figure 10. The difference in output power from typical to maximum VBATP is approx. 1.5 dBm which may

be neglected in most cases. It will at the utmost be of interest in applications that operate long distance line-of-sight, such as WLL.

5.3 Antennas

5.3.1 General Considerations

The antenna is the element that is responsible of radiating the radio frequency energy generated by the transmitter and has to capture the energy emitted by other transmitters to feed it to the receiver of the HW 86012 module. Antenna design is among the most important topics of a module integration. It has big influence on the coverage range of your product. With a poor antenna design or integration your product will not have the full coverage range of typical DECT equipment. Many insufficiencies observed at radio systems can be solved with changing a poor antenna with a good one.

Höft & Wessel provides a set of antennas and accessories that can be used in many applications. Depending on the physical constraints of your application it may require special antennas. In depth RF experience may be required in many cases. Contact Höft & Wessel if you need assistance with this topic. RF experts will be able to suggest antenna systems suitable for your application or develope application specific antennas. Most important parameters of antenna systems such as return loss and radiation diagrams can be measured to ensure antenna performance.

Basically, antennas shall be placed under the following considerations:

Internal antennas:

- may only be used with plastic housings. Take care as some plastics are conductive and will attenuate RF signals
- avoid shielding the antennas with metal objects or PCBs
- keep the antennas far from electronic signals and components
- be particularly careful with fast signals (like µC bus signals), if they come close to the antennas there is a risk of receiver sensitivity degradation by processor noise
- mismatching may occur if antenna comes close to metal parts an even too close to plastic materials, this situation must be considered when matching the antenna.

All antennas shall be placed

- so that few obstacle will be in the direct line of signals propagation
- away from large metal objects
- away from any electronic equipment
- so that they match the polarisation plane of their counterpart on the remote side in order to avoid polarisation losses. Omnidirectional antennas will usually provide omnidirectional characteristics in the plane perpendicular to the antenna axis, so they should usually be mounted vertically.
- so that the antennas omnidirectional radiation plane matches the wanted radio coverage, i.e. monolope or dipole antennas are usually required to be in a vertical position.

5.3.2 HW 86012 Antenna Ports and Recommendations

The HW 86012 module is equipped with one wire antenna on ANT1 port in standard configuration. This allows for easy integration and reasonable performance and is a good compromise in most cases. However, it is recommended to put the wire antenna in a vertical position to achieve an omnidirectional characteristic in the horizontal plane. Also, no metal parts, wires, circuit boards or components should be close to the antenna as this will significantly degrade the performance.

If the application requires a maximum performance or if it is not possible to reasonably position the wire antenna, seperated antennas shall be used that can easiliy be connected to the module's miniature coaxial connectors. Adapter cables are provided as accessories.

Using two antennas allows for antenna diversity. This feature significantly reduces the fading effect in multi-path environments. In this case two antennas shall be mounted in a distance of about 12..20 cm to each other. Usually both antennas shall provide omnidirectional characteristics and use the same polarisation (spatial diversity).

See command "SPANT" in HW 86012 Firmware Manual for detailed information on the antenna port configuration.

5.3.3 Antenna Gain

Both omnidirectional antennas and directional antennas provide an antenna gain, measured in dBi (which means dB over isotropic radiator).

Omnidirectional antennas provide an antenna gain in the range of 0 dBi (quarter-wavelength monopole over ground plane), 2dBi (half-wave dipole, coaxial antenna), 3..12 dBi (stacked elements). Directional antennas are mainly available as patch antennas or yagi antennas, providing gains up to more than 20 dBi.

Care must be taken if high gain antennas are used, as regulations limit the maximum antenna gain. Refer to the valid national regulations.

5.4 Range

The range of a wireless system is on one hand determined by the transmitter power, the receiver sensitivity and the gain of the antennas used. The significant factor is the attenuation of the radio path. This attenuation is a minimum in open space, i.e. a maximum range can be achieved here. In an industrial environment for example the radio path may be determined by huge obstacles which lead to strong attenuation of radio signals. In addition, reflections occur on objects within the radio path which lead to multi-path propagation. I.e. multiple signals that reach the receiver out of phase will lead to an additional attenuation referred to as fading.

Therefore the range that can be covered with Data-Unwired DECT systems depends on the application. However, typically values are:

- up to 60 m inside buildings
- up to 300 m outside buildings
- up to 1000 m and more under ideal conditions (line of sight, clear Fresnel zone)

Note that for extended range operation the receive time window, referred to as synchronisation window, must be increased by software. See command "SPSYWD" in HW 86012 Firmware Manual for details.

6. Accessories

6.1 Coaxial Adapter Cables

Adapter cables with U.FL plug to be attached to HW 86012 coaxial connectors and SMA bulkhead jack to attach an antenna or coaxial cable with SMA connector.

Connector A	Connector B	Length	Outer diameter	Order No
U.FL plug	SMA bulkhead jack (f)	100 mm	1.32 mm	100891
U.FL plug	SMA bulkhead jack (f)	200 mm	1.32 mm	100895

6.2 Antennas

Antennas with SMA connectors that can be attached to HW 86012 module using coaxial cable adapters.

Type	Description	Connector	Cable Length	Gain	Characteristics	Order No
Swivel Antenna	λ/2 dipole articul. 0-45-90° l = 155 mm d =13 mm	SMA (m)	-	2 dBi	vertical polarisation, omnidirectional	E18374
Panel Antenna	articulating wall mount patch antenna 15 x 10 x 6 cm beam width 75°	SMA (m)	1.5 m	7.5 dBi	vertical polarisation, directional	E18373

6.3 System Connector

Surface mount connector for host application, fits to HW 86012 system connector.

Pins	Grid	Pin length	Spacing host pcb - module pcb	Order No.
2 x 25	1.27 mm	10.0 mm	6.0 mm with bottom entry	E26056